



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,922	12/02/2003	Deva N. Pattanayak	VISH-8728	8797
7590	02/09/2006			EXAMINER FENTY, JESSE A
Eric J. Gash Wagner, Murabito & Hao LLP Third Floor Two North Market Street San Jose, CA 95113			ART UNIT 2815	PAPER NUMBER

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/726,922	PATTANAYAK ET AL.
	Examiner Jesse A. Fenty	Art Unit 2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 25 April 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-10 and 24-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-10, 24-26 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 11/14/05
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The rejection of claims 2 and 25, previously rejected under 35 U.S.C. 112, first paragraph, is withdrawn, based on Applicant's remarks filed 04/25/05.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-6, 8-10 and 24-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Saito et al. (US 2004/0195618 A1).

In re claim 1, Saito (esp. Fig. 1) discloses a semiconductor device, comprising:
a drain region (11);
a body region (12a) disposed above said drain region;
a gate region (24a-2) disposed within said body region;
a gate insulator region (23a; Fig. 12) disposed about a periphery of said gate region;

a plurality of source regions (13a) disposed along the surface of said body region proximate a periphery of said gate insulator region;

wherein a first portion of said gate region (24a-1) and a first portion of said gate insulator region are formed as a substantially parallel elongated structure;

wherein a second portion of said gate region (24a-2) and a second portion of said gate insulator region are formed as a normal-to-parallel structure;

wherein a first portion of said drain region overlaps said parallel structure; and

wherein a second portion of said drain region is separated from (by semiconductor region 14B) said normal-to-parallel structure.

In re claim 2, as best understood, Saito discloses the device of claim 1, wherein said device provides a low (decreased) gate-to-drain capacitance (section [0072], lines 13-17). The “on resistance,” as best understood is comparable to that of the instant application based on the similarity of structure between the Saito structure and that of Applicant’s Prior Art (Fig. 2), described on pp. 6, lines 8-12) of Applicant’s specification.

In re claim 3, Saito discloses the device of claim 1, wherein said closed cell MOSFET provides a reduced gate-to-drain capacitance gate-to-source capacitance ratio. This claim is met by the prior art Saito for the same reasons as the instant application, in that a low gate-to-drain capacitance will produce a high gate-to-source capacitance (Applicant’s specification pp. 15, lines 5-6). This, in turn, produces the claimed reduced ratio (pp. 15, lines 11-13). There is no reason why this same result will not be present with the structure of the prior art Saito.

In re claim 4, Saito discloses the device of claim 1, wherein said overlap of said first portion of said drain region and said parallel elongated structure comprises an extension of said drain region.

In re claim 5, Saito discloses the device of claim 1, wherein said separation of said second portion of said drain region and said normal-to-parallel elongated structure comprises a well (14B) of said body portion.

In re claim 6, Saito discloses the device of claim 1, wherein said body region (12a) and said plurality of source regions (13a) are electrically coupled together.

In re claim 8, Saito discloses the device of claim 1, wherein said drain region comprises:

a first drain portion (15) having a high doping concentration (section [0083], line 5); and

A second drain portion (11), having a low doping concentration (section [0083], line 8), disposed between said body region (12) and said first drain region.

In re claim 9, Saito discloses the device of claim 8. The limitation, "wherein said second drain portion increases ... TMOSFET" is a recitation of the intended use of the claimed device. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art.

In re claim 10, Saito discloses the device of claim 8, wherein said first portion of said drain region comprises a heavily n-doped semiconductor; and

said second portion of said drain region comprises a lightly n-doped semiconductor.

 In re claim 24, Saito (esp. Fig. 1) discloses a semiconductor device, comprising:
 a plurality of open gate-drain regions (with gate 24a-2) arranged in a first plurality of parallel regions; and
 a plurality of closed gate-drain regions (with gate 24-1) arranged in a second plurality of parallel regions normal to said open gate-drain regions.

 In re claim 25, as best understood, Saito discloses the device of claim 24, wherein said device provides a low (decreased) gate-to-drain capacitance (section [0072], lines 13-17). The “on resistance,” as best understood is comparable to that of the instant application based on the similarity of structure between the Saito structure and that of Applicant’s Prior Art (Fig. 2), described on pp. 6, lines 8-12) of Applicant’s specification.

 In re claim 26, Saito discloses the device of claim 24, wherein said closed cell MOSFET provides a reduced gate-to-drain capacitance gate-to-source capacitance ratio. This claim is met by the prior art Saito for the same reasons as the instant application, in that a low gate-to-drain capacitance will produce a high gate-to-source capacitance (Applicant’s specification pp. 15, lines 5-6). This, in turn, produces the claimed reduced ratio (pp. 15, lines 11-13). There is no reason why this same result will not be present with the structure of the prior art Saito.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saito as applied to claim 1 above, and further in view of Darwish et al. (US 2003/0062570 A1).

In re claim 7, Saito discloses the device of claim 1, whrein;
said drain region (11, 15) comprises an n-doped semiconductor (section [0082], lines 3-4);
said body region (12) comprises a p-doped semiconductor (section [0080]);
said gate insulator region (23a) comprises an oxide (section [0081]);
said plurality of source regions (13a) comprises a heavily n-doped semiconductor (section [0079], line 13), but does not expressly disclose said gate region comprising a heavily doped n-doped semiconductor. Darwish (esp. Fig. 3) discloses a heavily doped semiconductor polysilicon region (14) filling the gate trench (section [0024]). Darwish does not expressly disclose said gate layer comprising an N-type semiconductor. However, it would have been obvious for one skilled in the art at the time of the invention to select an N-type impurity rather than a P-type impurity for the gate electrode for the purpose, for example, of enhancing the conductivity of the vertical channel region. This would be the obvious choice because both the source and drain regions are also N-type.

Response to Arguments

1. Applicant's arguments filed 04/25/05 have been fully considered but they are not persuasive.
 - a. Applicant asserts that Saito does not teach or suggest the limitation, "a second portion of said drain region is separated from said normal-to-parallel structure" as recited by Claim 1. Applicant asserts that all drain regions overlap the parallel structure. Applicant quotes language of Saito such that each gate electrode has a "constant depth" and a "larger depth" than the base layer (12a). Applicant asserts that Saito is silent regarding the drain region being separated from the structure.
 - i. If a prior art reference does not expressly disclose in the specification the teachings in the same manner claimed by the applicant, the drawings are part of the prior art disclosure and can be interpreted in light of the specification to read on the pending claims.
 - ii. Here, Saito discloses a layer (14B) which acts to "separate" the normal-to-parallel structure from the drain regions. This layer was cited in Examiner's rejection mailed 01/26/05 as the layer that "separates" the two claimed layers. The patent office has the duty to interpret the claims broadly, where the claims do not provide such specificity.
 - iii. Applicant's arguments about the "depth" of the gate regions does not relate to the pending claims. Independent claim 1 does not claim the depth of the gate regions. Claim 1 simply says the one gate region is

"separated" from the drain region. Such limitation is met by the disclosure of Saito, even if not described in Saito's specification exactly the same as claimed.

iv. Therefore, the rejection of claim 1 and pending claims are maintained.

b. Regarding claim 24, applicant asserts that Saito does not teach or suggest "a plurality of open gate-drain regions arranged in a first plurality of parallel regions."

v. On the contrary, the open gate-drain regions are the gate-drain regions (24a-2) coincide with the structure of the open gate-drain regions (450) and closed gate-drain regions (451) disclosed by applicant, especially in Fig. 4 of applicant's specification. As interpreted by the examiner, the defining characteristic between applicant's two gate regions is the impurity layer (450) below gate the gate region (422).

(1) Likewise, Saito disclose am impurity layer (14B) below the gate region (24a-2). Therefore, the device of Saito reads on the claims.

vi. The fact that Saito is "silent" about "open gate-drain regions" does not mean that the disclosure does not read on the claims. A prior art disclosure need not recite each and every element in exactly the same manner as a pending claim to anticipate the pending claim.

vii. Also, applicant refers to the doping concentration of the separation layer (14B). However, there is no reference in claim 24 to the doping concentration of the layer separating the gate from the drain.

c. For these reasons, the rejection based on Saito is maintained.

Conclusion

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty
Examiner
Art Unit 2815



KENNETH PARKER
SUPERVISORY PATENT EXAMINER